Please amend page 13, line 21 as follows:

In write and erase operations, when a voltage as shown in tables 3 and 4 is applied to n-type well region 2a and one source/drain impurity diffused region 11 (or the other source/drain impurity diffused region 11), a depletion layer is formed at pn junctions between n-type well region 2a and p-type semiconductor substrate 1 and between one source/drain impurity diffused region 11 (or the other source/drain impurity diffused region 11) and the P-type well region 12. As the depletion layer extends further, leakage current associated with the punch-through increases.